



偉詮電子股份有限公司  
**Weltrend Semiconductor, Inc.**

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**WT7527V**  
**PC POWER SUPPLY SUPERVISOR**  
**Data Sheet**

**Version 1.01**

**July 9, 2010**

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## GENERAL DESCRIPTION

The WT7527V provides protection circuits, power good output (PGO), fault protection latch (FPOB), and a protection detector function (PSONB) control. It can minimize external components of switching power supply systems in personal computer.

The Over Voltage Detector (OVD) monitors VX, V33, V5, V12A and V12B input voltage level. The Under Voltage Detector (UVD) monitors V33, V5, V12A and V12B input voltage level. The Over Current Detector (OCD) monitor I33&V33, I5&V5, I12A&V12A and I12B&V12B input current sense. The pin VX provides an extra protection function. When OVD or UVD or OCD or VX detect the fault voltage level, the FPOB is latched HIGH and PGO go low. The latch can be reset by PSONB go HIGH. There is 4 ms delay time for PSONB turn off FPOB.

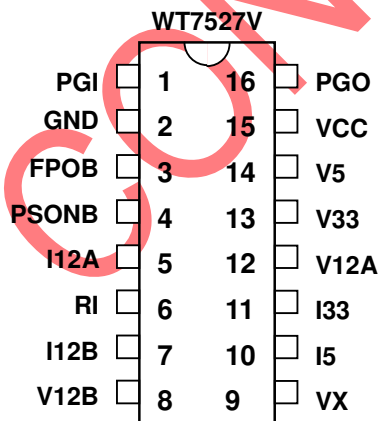
When OVD and UVD and OCD detect the right voltage level, the power good output (PGO) will be issue.

## FEATURES

- The Over Voltage Detector (OVD) monitors VX, V33, V5, V12A and V12B input voltage.
- The Under Voltage Detector (UVD) monitors V33, V5, V12A and V12B input voltage.
- The Over Current Detector (OCD) monitors I33&33, I5&V5, I12A&V12A and I12B&V12B input pins.
- The VX > 1.2V provide an extra protection.
- Both of the power good output (PGO) and fault protection latch (FPOB) are Open Drain Output.
- 75 / 600 ms time delay for UVD / OCD / VX .
- 300 ms time delay for PGO.
- 38 ms for PSONB input signal De-bounce.
- 14 us for OVD internal signal De-bounce.
- 60 us for UVD / VX internal signal De-bounce.
- 20 ms for OCD internal signal De-bounce.
- 73 us for PGI internal signal De-bounce.
- 4 ms for PSONB turn-off FPOB.

## PIN ASSIGNMENT AND PACKAGE TYPE

### Pin assignment



## ORDERING INFORMATION

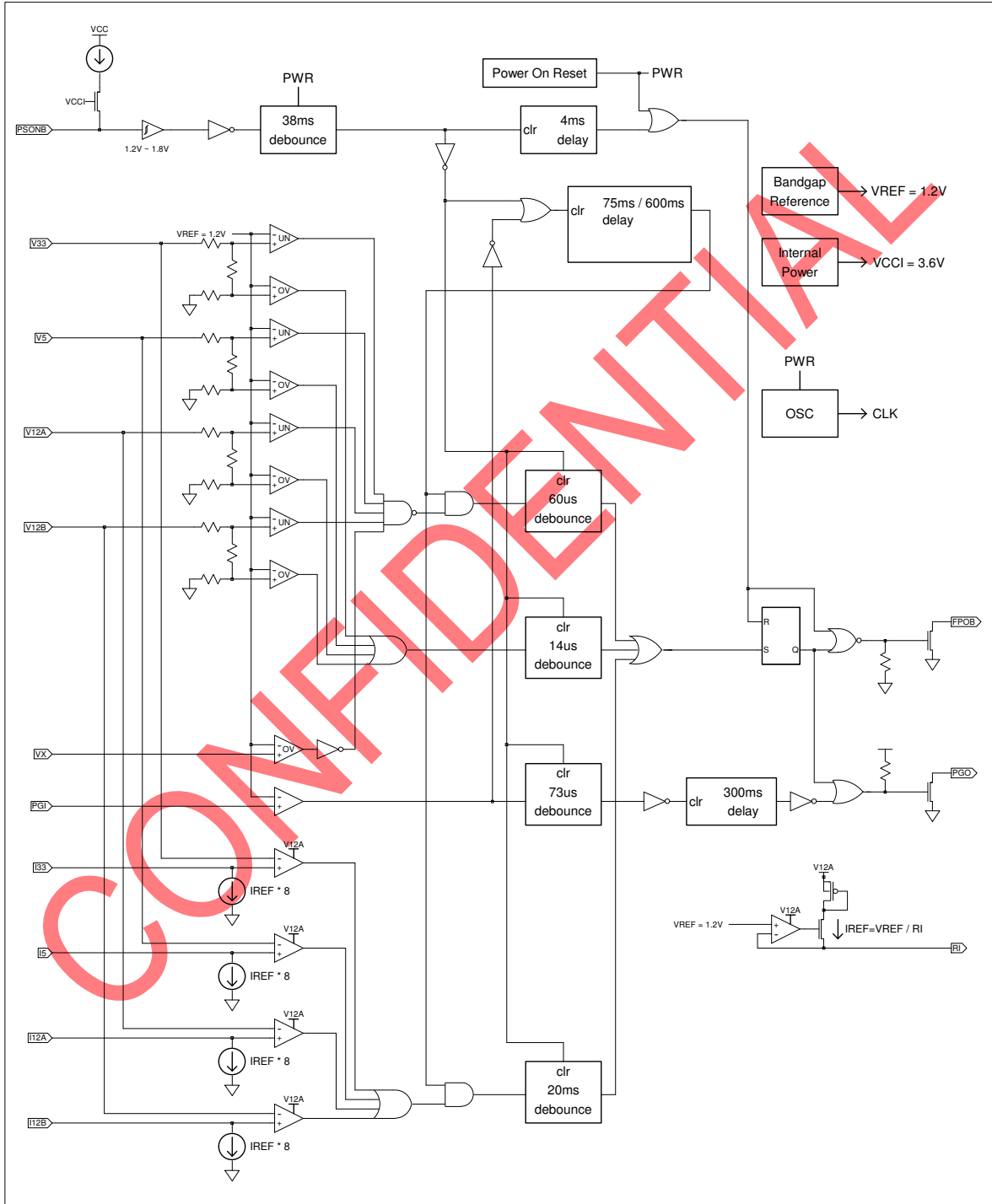
Part Number	Package Type	Note
WT7527V-NG160WT-T1	16-Pin Plastic DIP, Halogen-free	Green Package
WT7527V-SG160WT-T1	16-Pin Plastic SOP, Halogen-free	Green Package

## PIN DESCRIPTION

Pin Name	I/O	Description
PGI	I	Power good input signal pin
GND	P	Ground
FPOB	O	Fault protection output pin, open drain output
PSONB	I	On/Off switch input
I12A	I	12VA over current protection sense input
RI	I	Current sense adjust input
I12B	I	12VB over current protection sense input
V12B	I	12VB over voltage & under voltage & over current sense input pin
VX	I	Extra protection sense input
I5	I	5V over current protection sense input
I33	I	3.3V over current protection sense input
V12A	I	12VA over voltage & under voltage & over current sense input pin
V33	I	3.3V over voltage & under voltage & over current sense input pin
V5	I	5V over voltage & under voltage & over current sense input pin
VCC	I	Power supply
PGO	O	Power good output signal pin, open drain output

## BLOCK DIAGRAM

### WT7527V



**ABSOLUTE MAXIMUM RATINGS**

Parameter		Min.	Max.	Unit
Supply voltage, VCC, V12A		-0.3	15	V
Input voltage	PGI, PSONB	-0.3	VCC + 0.3 (Max. 7V)	V
	V5, I5, V33, I33		V12A + 0.3 (Max. 7V)	V
	I12A, V12B, I12B		V12A + 0.3 (Max. 15V)	V
Output voltage	PGO	-0.3	VCC + 0.3 (Max. 7V)	V
	FPOB	-0.3	15	V
Operating temperature		-20	85	°C
Storage temperature		-55	150	°C

\*Note: Stresses above those listed may cause permanent damage to the devices

**RECOMMENDED OPERATING CONDITIONS**

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC			3.8	5	15	V
Input voltage	PGI, PSONB, V5, V33				7	V
	V12A, V12B				15	V
Output voltage	PGO				7	V
	FPOB				15	V
Output sink current	FPOB	0.3V			10	mA
	PGO	0.3V			10	mA
Supply voltage rising time			1			mS
Output current for RI		RI	10		65	uA
Operating free-air Temp.		Ta	-20		85	°C

**ELECTRICAL CHARACTERISTICS, at Ta=25°C and VCC=5V.**
**Over Voltage Detection**

Parameter		Condition	Min.	Typ.	Max.	Unit
Over voltage threshold	V33		3.8	3.9	4.0	V
	V5		5.6	5.8	6.0	V
	V12AB		13.5	13.85	14.2	V
	VX	Use UVD timing	1.176	1.20	1.224	V
I <sub>LEAKAGE</sub> Leakage current (FPOB)		V(FPOB) = 5V		5		uA
V <sub>OL</sub> Low level output voltage (FPOB)		I <sub>sink</sub> = 10mA			0.3	V

**PGI and PGO**

Parameter		Condition	Min.	Typ.	Max.	Unit
Under voltage threshold	V33		2.8	2.9	3.0	V
	V5		4.2	4.4	4.6	V
	V12AB		9.5	10	10.5	V
Input threshold voltage(PGI)			1.176	1.20	1.224	V
I <sub>LEAKAGE</sub> Leakage current(PGO)		PGO = 5V		5		uA
V <sub>OL</sub> Low level output voltage(PGO)		I <sub>sink</sub> = 10mA			0.3	V
Offset Voltage of OCP comparators			-3		3	mV



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## PSONB

Parameter	Condition	Min.	Typ.	Max.	Unit
Input pull-up current	PSONB= 0V		160		uA
High-level input voltage		1.8			V
Low-level input voltage				1.2	V

## TOTAL DEVICE

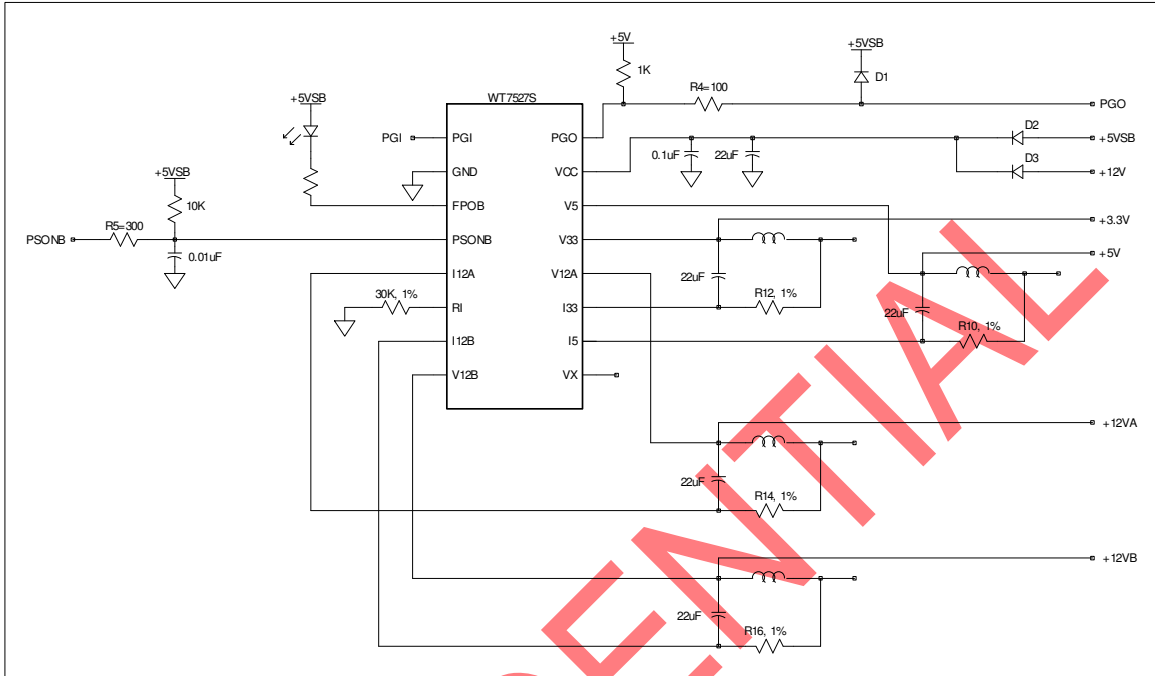
Parameter	Condition	Min.	Typ.	Max.	Unit
Icc Supply current	PSONB= 5V			1	mA
Vcc operation start up voltage		3.2	3.4	3.6	V
Vcc under lockout voltage		2.8	3.0	3.2	V
Supply voltage rising time		1			mS

## SWITCHING CHARACTERISTICS, at Ta=-20°C ~85°C

Parameter	Condition	Min.	Typ.	Max.	Unit
PGI to PGO Delay Time	Td1	200	300	400	mS
Internal UVD/OCD delay time at power on mode (Note1)	Td2	49	75	100	mS
	Td2-1	392	600	800	mS
Internal UVD/OCD delay time at normal mode (Note1)	Td2	49	75	100	mS
		PGI < 1.2V	Disable UVD/OCD check		
PGO to FPOB Delay Time	Td3	2	4	6	mS
Under Voltage Delay Time	Td4	40	60	81	μS
Over Current Delay Time	Td5	13	20	27	mS
Over Voltage Delay Time	Td6	9	14	19	uS
VX Delay Time	Td7	40	60	81	μS
PSONB De-bounce Time	Tb1	24	38	52	mS
PGI De-bounce Time	Tb2	47	73	100	μS

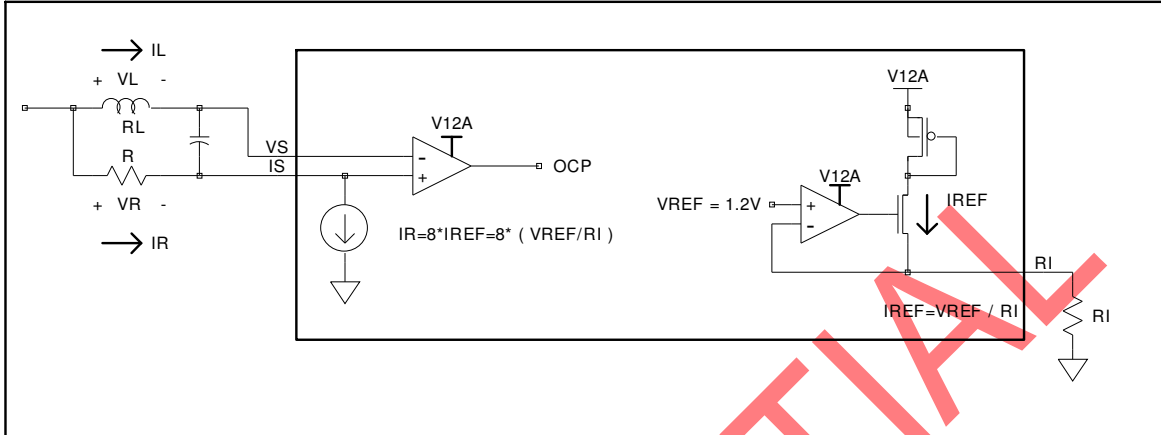
NOTE1: When FPOB go low, the WT7527V enter the power on mode at first. And then jump to normal mode when the UVD and OCD are right.

## APPLICATION CIRCUIT



- NOTE1: The series resistor R5 at PS0NB can not be omitted. ( R5 = 300Ω is suggested )
- NOTE2: The series resistor R4 = 100Ω and diode D1 at PGO is suggested. If not, should add on testing-board or burning-board at least.
- NOTE3: Supply and signal must pass through the capacitor first before into IC.
- NOTE4: The capacitor 0.1μF & 22μF at VCC is suggested. And diode D2 & D3 at VCC can not be omitted
- NOTE5: When VCC use single power, diode D2 at VCC can not be omitted.

## APPLICATION NOTE



When the load current increased, the voltage (VL) cross the inductor is increased. And when inductor voltage exceeds the resistor voltage (VR), the OCP is active.

Sometimes power-on or load dynamics will cause false output of over-current detection. It can be solved by connecting a capacitor between VS pin and IS pin. In typical case,  $C \geq 1\mu\text{F}$  is suggested.

OCP point can be calculated by the following equation:

Let  $VR = VL$

$$R \times IR = RL \times IL$$

$$\therefore IR = 8 \times IREF = 8 \times \frac{VREF}{RI}$$

$$\therefore R = \frac{RL \times IL}{8 \times \frac{VREF}{RI}}$$

For example :

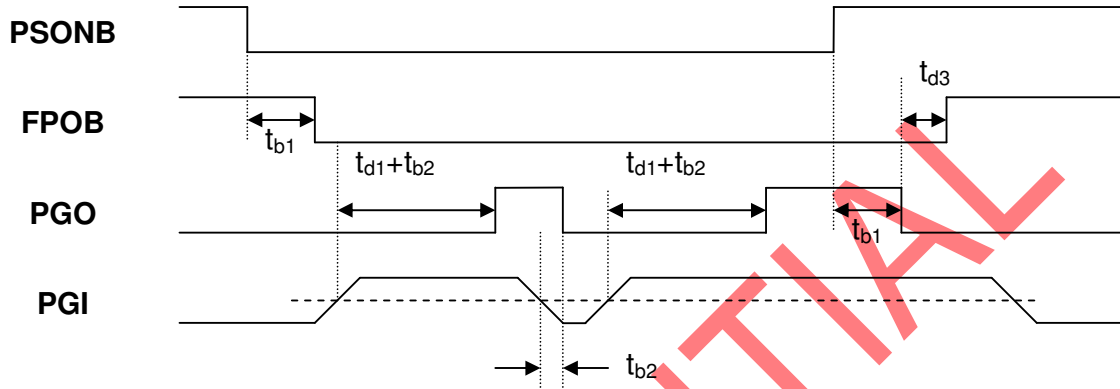
Assume  $RI=30\text{K}\Omega$ ,  $RL=5\text{m}\Omega$ , OCP  $IL=20\text{A}$ .

$$\begin{aligned} \text{Sol : } R &= (IL * RL) / (8 * IREF) \\ &= (20\text{A} * 5\text{m}\Omega) / \{8 * (1.2\text{V} / 30\text{K}\Omega)\} \\ &= 312.5\Omega \end{aligned}$$



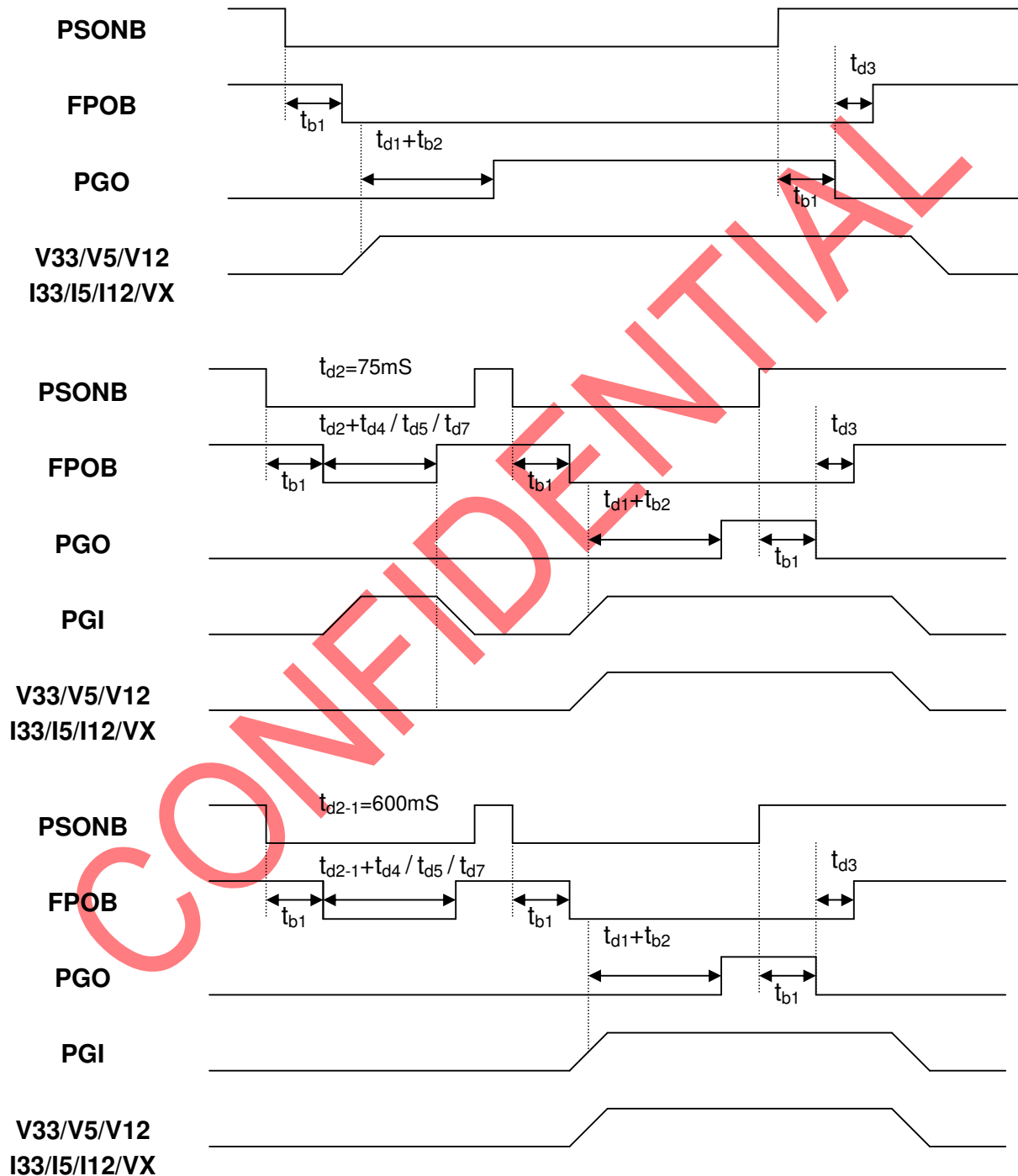
**APPLICATION TIMMING**

**1.) PGI (UNDER\_VOLTAGE) :**

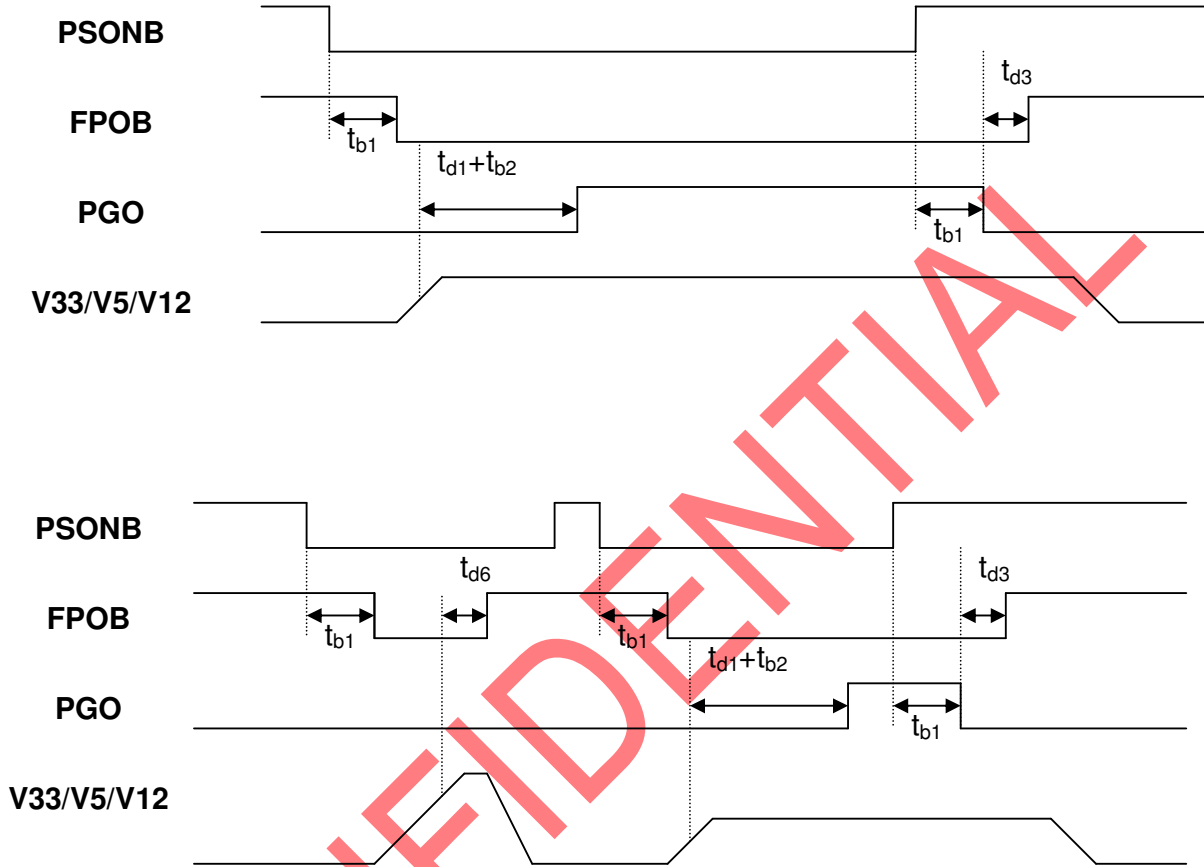


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2.) V33, V5, V12 (UNDER\_VOLTAGE) or I33, I5, I12 (OVER\_CURRENT) or VX (OVER\_VOLTAGE) :

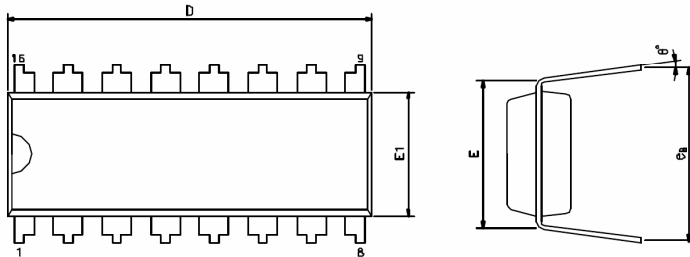


3.) V33, V5, V12 (OVER\_VOLTAGE) :



## MECHANICAL INFORMATION

### PLASTIC DUAL-IN-LINE PACKAGE

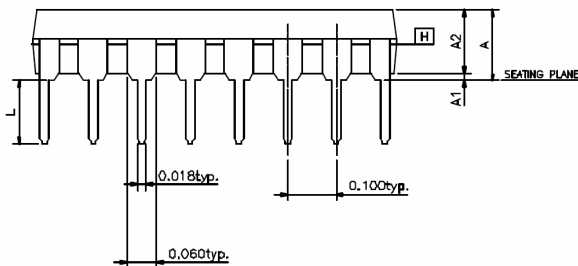


SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	0.735	0.755	0.775
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e <sub>B</sub>	0.335	0.355	0.375
Ø	0	7	15

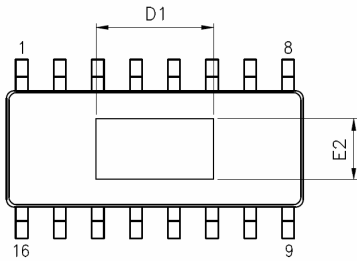
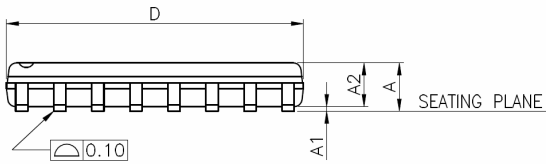
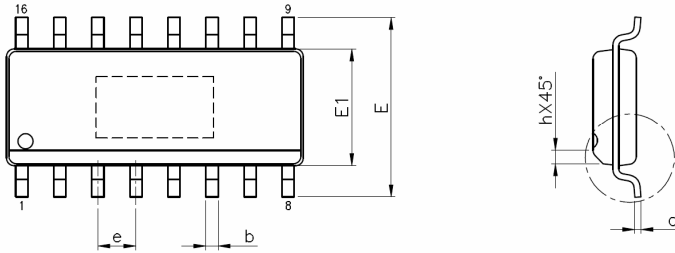
UNIT : INCH

**NOTES:**

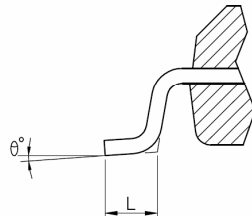
1. JEDEC OUTLINE : MS-001 BB
2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. e<sub>B</sub> IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.



## PLASTIC SMALL-OUTLINE PACKAGE



(THERMAL VARIATIONS ONLY)



SYMBOLS	STANDARD		THERMAL	
	MIN.	MAX.	MIN.	MAX.
A	—	1.75	—	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	—	1.25	—
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	9.90 BSC		9.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
$\theta^\circ$	0	8	0	8

UNIT : mm

### THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
95X18E	1.68	2.41	3.86	4.57

UNIT : mm

### NOTES:

1. JEDEC OUTLINE : MS-012 AC REV.F (STANDARD)  
MS-012 BC REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS, INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.